CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method of operating an imager, comprising:

generating charges with a photosensor;

transferring charges from said photosensor to a storage node;

selectively increasing the charge storage capacity of said node; and

producing an electrical signal in response to charges transferred to said node.

2. The method of claim 1, wherein said act of selectively increasing the charge storage capacity of said node comprises selectively activating a gate capacitor coupled to said node.

3. The method of claim 2, wherein activating the gate capacitor operates to eliminate substantially all charge in the photosensor during said transfer.

4. The method of claim 1, wherein said act of selectively increasing the charge storage capacity of said node occurs prior to said charge transfer.

5. The method of claim 1, wherein the imager is a CMOS imager.

6. The method of claim 1, wherein the imager is a CCD imager.

7. An integrated circuit comprising:

a substrate; and

a pixel array, each pixel in the pixel array comprising:

a photosensor operable to receive photon energy and convert the photon energy to photoelectric charge;

a floating diffusion region for receiving the photoelectric charge; and

at least one gate capacitor connected to the floating diffusion region, each gate capacitor operable to increase a charge storage capacitance of the floating diffusion region.

8. The integrated circuit of claim 7, wherein said photosensor is selected from the group consisting of a photodiode, photogate, and a photoconductor.

9. The integrated circuit of claim 7, wherein said at least one gate capacitor comprises a lower capacitor plate electrically coupled to the floating diffusion region and an upper capacitor plate connected to a contact.

10. The integrated circuit of claim 7, wherein said at least one gate capacitor is located between a transfer gate and a reset gate.

11. The integrated circuit of claim 7, wherein said at least one gate capacitor is formed over a portion of the floating diffusion region.

12. The integrated circuit of claim 7, wherein the pixel array is a CMOS pixel array.

13. The integrated circuit of claim 7, wherein the pixel array is operated by timing and control circuitry.

14. The integrated circuit of claim 13, wherein the timing and control circuitry generates a timing signal to selectively operate the at least one gate capacitor.

15. A method of forming a pixel, comprising:

forming a photosensor on a substrate, said photosensor detecting and storing photon energy;

forming a transfer gate on said substrate;

forming a floating diffusion region on said substrate; and

forming a gate capacitor over said substrate, the gate capacitor being connected to the floating diffusion region.

16. The method of claim 15, wherein the gate capacitor is formed over a portion of the floating diffusion region.

17. A pixel of an imager, said pixel comprising:

a photosensing region which receives incident light and generates photoelectric charges;

a diffusion region for receiving photogenerated charges from said photosensing region; and

at least one capacitor switchably operable to increase capacitance of said diffusion region.

18. The pixel of claim 17, wherein each capacitor is a gate capacitor.

19. A method of achieving high conversion gain in an image sensor, said method comprising:

activating at least one photosensor at or beneath a surface of a substrate, wherein each photosensor operates to detect photon energy and convert said photon energy to photoelectric charge;

activating a gate capacitor to increase charge storing capacitance of a storage node;

transferring said photoelectric charge generated in each photosensor to said storage node; and

converting said photoelectric charge at said storage node to an electrical signal.

20. An image pixel array in an imaging device, each pixel in the pixel array comprising:

a photosensor operable to receive photon energy and convert the photon energy to photoelectric charge;

a floating diffusion region for receiving the photoelectric charge; and

at least one gate capacitor connected to the floating diffusion region, each gate capacitor being selectively operable to increase a charge storage capacitance of the floating diffusion region.

21. The image pixel array of claim 20, wherein each photosensor is selected from the group consisting of a photodiode, photogate, and photoconductor.

22. A CMOS imager system, comprising:

a processor; and

an imaging device coupled to said processor, said imaging device comprising:

a pixel array, each pixel in the pixel array comprising:

a photosensor operable to receive photon energy and convert the photon energy to photoelectric charge;

a floating diffusion region for receiving the photoelectric charge; and

at least one gate capacitor connected to the floating diffusion region, each gate capacitor being selectively operable to increase a charge storage capacitance of the floating diffusion region.

23. The imager system of claim 22, further comprising timing and control circuitry for operation of the pixel array.

24. The imager system of claim 23, wherein the timing and control circuitry generates a timing signal to selectively operate the at least one gate capacitor.

25. The imager system of claim 22, wherein the at least one gate capacitor increases total charge capacitance such that said imager system has increased responsiveness to low light and high light signal conditions.

26. A CCD imager comprising:

a register for inputting and outputting photo-generated charge;

a storage node, connected to receive the photo-generated charge from said register; and

at least one gate capacitor connected to the storage node, each gate capacitor being selectively operable to increase a charge storage capacitance of the storage node.

27. A CCD imager system, comprising:

a processor; and

a CCD imager coupled to said processor, said CCD imager comprising:

a register for inputting and outputting photo-generated charge;

a storage node, connected to receive the photo-generated charge from said register; and

at least one gate capacitor connected to the storage node, each gate capacitor being selectively operable to increase a charge storage capacitance of the storage node.